

Optimal and Heuristic Global Code Motion for Minimal Spilling

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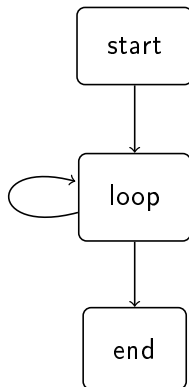
Solve **global code motion** and **register allocation** as an integrated problem.

Given: Scheduling for minimal spilling is good.

Hypothesis: Global code motion for minimal spilling might be good.

Global code motion

```
start:
  j0 := 0
  a := read()
loop:
  j1 :=  $\phi(j0, j2)$ 
  b := a + 1
  j2 := j1 + b
  c := f(a)
  compare j2 < c
  d := j2  $\times$  2
  blt loop
end:
  return d
```



Global code motion

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start:
  j0 := 0
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loop:
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  d := j2  $\times$  2  partially dead
  blt loop
end:
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Global code motion

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start:

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Global code motion

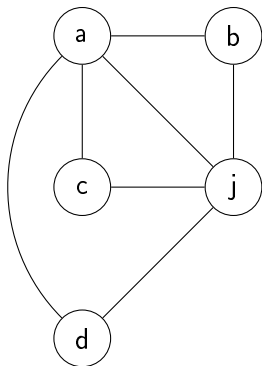
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live range of b

```
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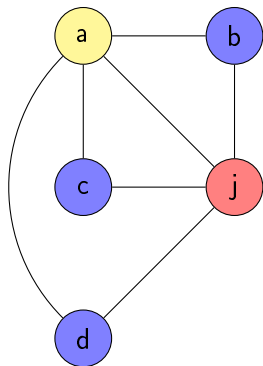
Register allocation: conflict graphs

original program



Register allocation: conflict graphs

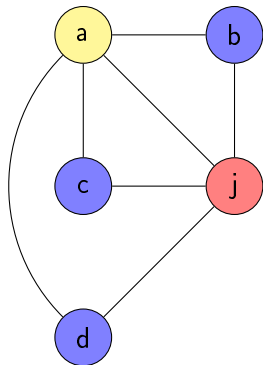
original program



allocation to 3 registers possible

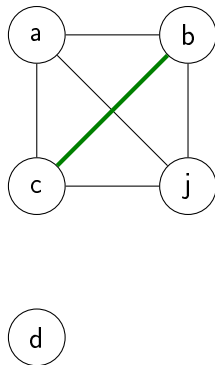
Register allocation: conflict graphs

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allocation to 3 registers possible

after global code motion



not 3-colorable!

Compute code motions and overlaps

All avoidable overlaps

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start:
i0:  j0 := 0
i1:  a := read()
loop:
i2:  j1 :=  $\phi(j0, j2)$ 
i3:  b := a + 1
i4:  j2 := j1 + b
i5:  c := f(a)
i6:  compare j2 < c
i7:  d := j2  $\times$  2
i8:  blt loop
end:
i9:  return d
```

Pair	Overlapping placement
a, d	i7 in loop
b, c	i3 in start
b, d	i3 in start, i7 in loop
b, j0	i3 in start
b, j2	i3 in start
c, d	i7 in loop, i7 before i6
d, j2	i7 in loop

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i7 in loop: overlap!

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i7 not in loop: no overlap

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i3 in start, i7 in loop: overlap!

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i3 not in start: no overlap

Compute code motions and overlaps

All avoidable overlaps

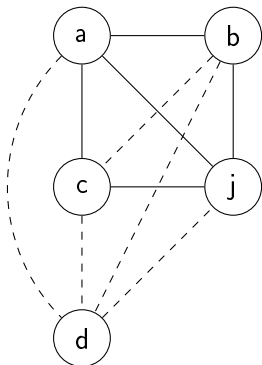
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i7 not in loop: no overlap

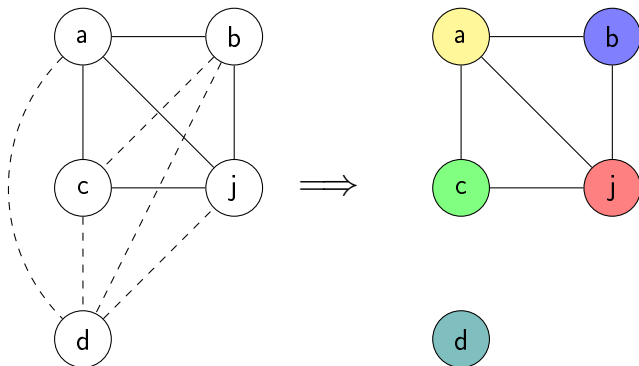
Register allocation

Conflict graph with special edges for **avoidable** overlaps. Allocate to different registers **if possible**.



Register allocation

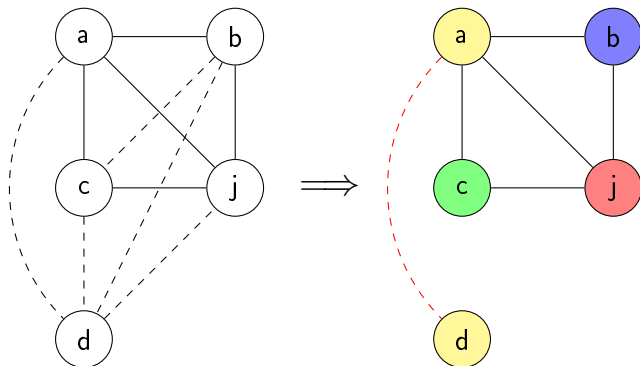
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5 registers: easy allocation

Register allocation

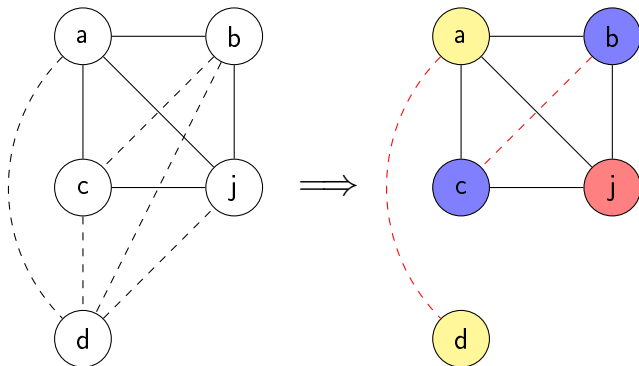
Conflict graph with special edges for **avoidable** overlaps. Allocate to different registers **if possible**.



4 registers: place instruction i7 in block end to avoid overlaps

Register allocation

Conflict graph with special edges for **avoidable** overlaps. Allocate to different registers **if possible**.



3 registers: place i3 in loop and i7 in end

There is just one problem. . .

Real-world programs have conflicting avoidable overlaps:

Pair	Overlapping placement
v1, v9	instruction 23 in block 0
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	⋮

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v1, v9	instruction 23 in block 0
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	must be in block 0 or 1!
	⋮

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Real-world programs have conflicting avoidable overlaps:

Pair	Overlapping placement	Overlapping schedule
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	⋮	

→ Must select a **subset** of reuses.

Which subset to choose?

To minimize spilling, choose valid subset with largest total savings in spill costs.

Intuition: Hypergraph Maximum Independent Set

Hypergraph $\langle V, H \rangle$ with:

- Vertices V : reuse candidate pairs
- Hyperedges H : minimal conflicting sets

Select maximum subset of V that does not contain any $h \in H$.

Idea: Avoid overlaps with larger spill costs.

Greedy heuristic selection

- Sort candidates by descending spill costs
- For each candidate:
 - If no conflict:
 - Add candidate to selected set
 - Commit to code motions for candidate

If greedy approach causes too many overlaps: use given schedule.

Can we do better than the greedy heuristics?

Integer linear programming formulation

Variables:

$select_c$ Select candidate c with savings w_c

$place_{i,b}$ Place instruction i in block b

... Variables for relative ordering of instructions

Objective function:

$$\text{maximize } \sum_c w_c select_c$$

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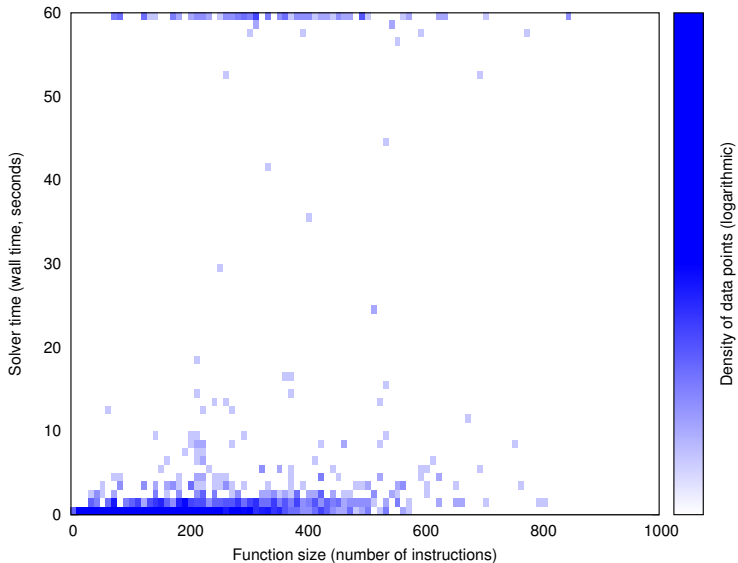
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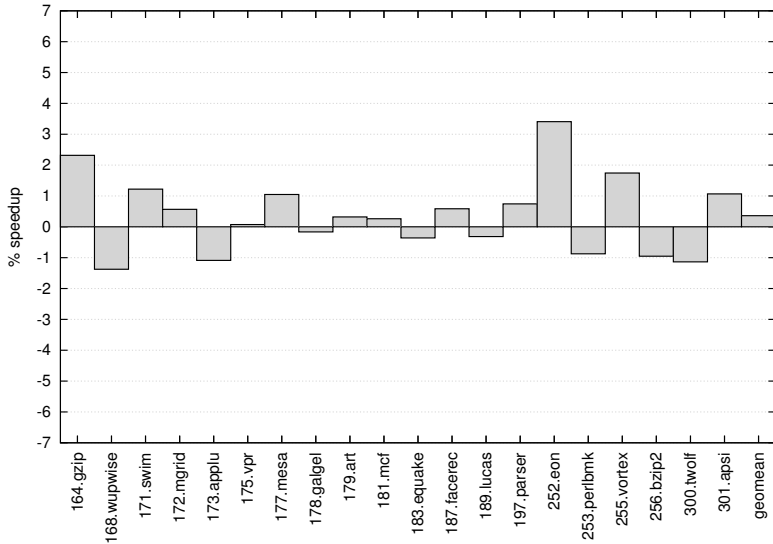
Objective function:

$$\text{maximize } \sum_c w_c select_c + \sum_i \sum_b place_{i,b}$$

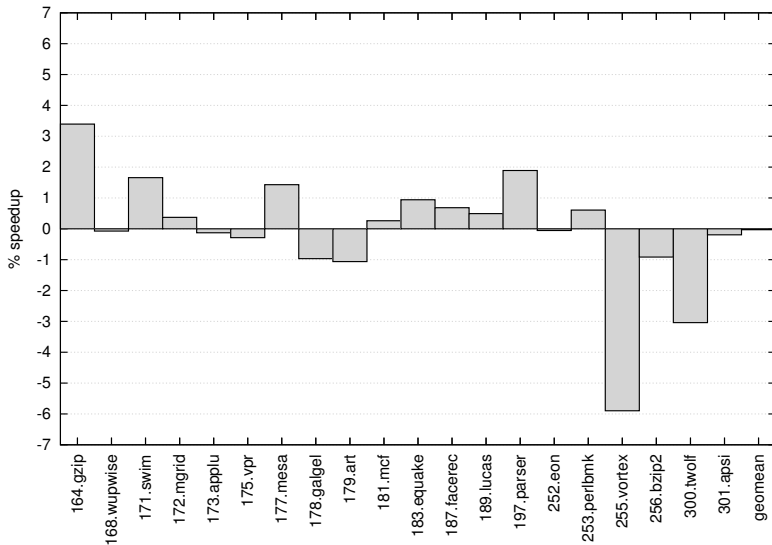
CPLEX solver time



Results: Greedy heuristics



Results: Optimal (ILP)



Some research directions

- More freedom for code motion:

$$\text{maximize } \sum_c w_c \text{select}_c + \beta \sum_i \sum_b \beta_b \text{place}_{i,b}$$

- Impact of solver time limit
- Other heuristics

Summary

- Integrate code motion and register allocation by letting the allocator choose necessary code motions.
- Speedups up to 4% 😊
- ...but no improvement on average 😞

Conclusion: Code motion for **minimal** spilling seems too restrictive.

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Thank you!

This work was supported by the Austrian Science Fund (Fonds zur Förderung der wissenschaftlichen Forschung) under contract P21842, *Optimal Code Generation for Explicitly Parallel Processors*.